DIGITAL SIGNAL PROCESSOR WITH PARALLEL ARCHITECTURE

Abstract of the Disclosure

A digital signal processor is designed to execute variable-sized instructions that may include up to N elementary instruction codes. The processor comprises a memory program comprising I individually addressable, parallel-connected memory banks in which the codes of a program are recorded in an interlaced fashion, and a circuit for reading the program memory arranged to read a code in each of the I memory banks during a cycle for reading an instruction. A cycle for reading an instruction in the program memory includes reading a sequence of codes that includes the instruction code or codes to be read and can also include codes, belonging to a following instruction, that are filtered before the instruction is applied to execution units. The program memory of the digital signal processor does not include any no-operation type codes.